ABSTRACT OF THE DISCLOSURE

A PLL circuit for generating a clock signal using a reference signal, the frequency of which is relatively low. The PLL circuit includes a first loop circuit for generating a first clock signal which is synchronized with a first reference signal. A second loop circuit generates a second clock signal which is synchronized with a second reference signal. The frequency of the second reference signal is sufficiently lower than the frequency of the first reference signal. The first reference signal is compared with the first clock signal to generate a first control voltage. The second reference signal is compared with the second clock signal to generate a second control voltage. The second loop circuit generates the second clock signal in accordance with the first control voltage and the second control voltage.